80 CHANNEL SEGMENT DRIVER FOR LCD DOT MATRIX LCD

The KS0104 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology. This device consists of 80 bit bidirectional shift register, 80 bit data latch and 80 bit driver (refer to fig 1).

100 QFP

FUNCTION

- Dot matrix LCD segment driver with 80 channel output
- Input/Output signal
  - Input: 4 bit parallel display data, control pulse from controller and bias voltage (V_1, V_3, V_4, V_{EE})
  - Output; 80 channel waveform for LCD driving.
- Power down function to make power consumption low.

FEATURES

- Power supply voltage: $+5V \pm 10\%$
- Supply voltage for display: $-8 \sim -28V (V_{EE}-V_{DD})$
- Parallel data processing (4 bit)
- Applicable LCD duty: $\dfrac{1}{64} \sim \dfrac{1}{256}$
- Interface

driver	
COM	**SEG (cascade)**
KS0083, KS0103	Other KS0104

- High voltage CMOS process
- 100 QFP and bare chip available.

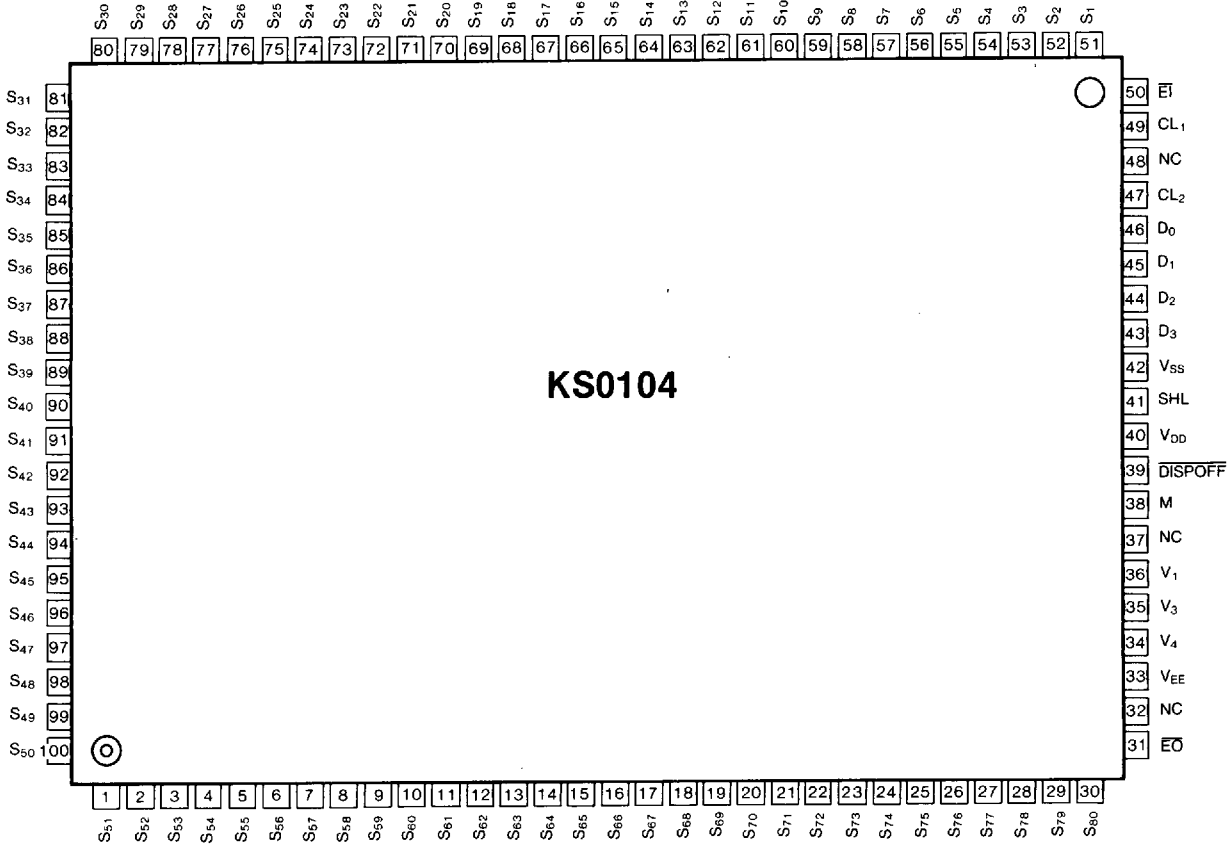## BLOCK DIAGRAM
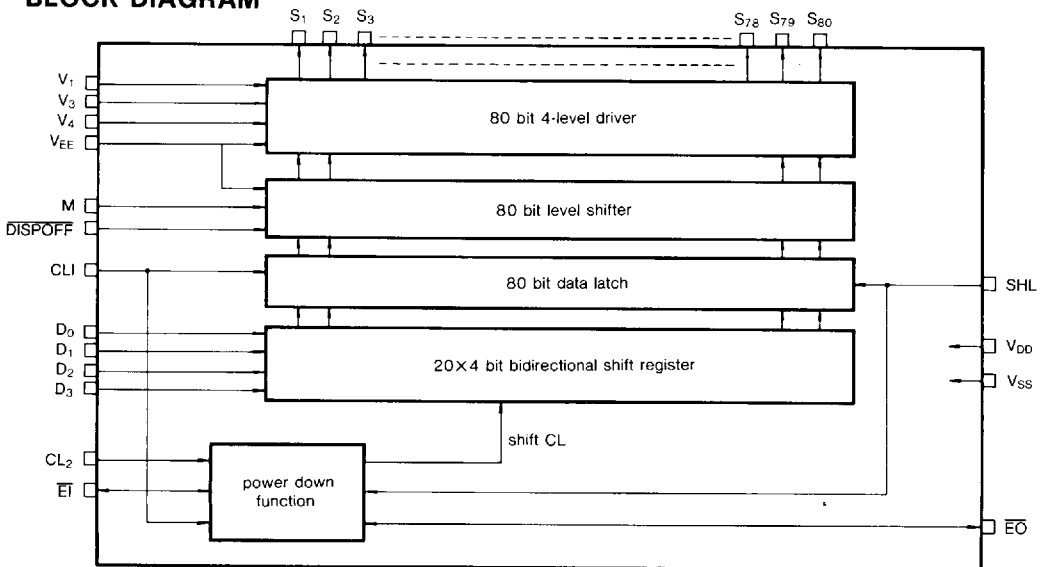
Fig 1. KS0104 Functional block diagram

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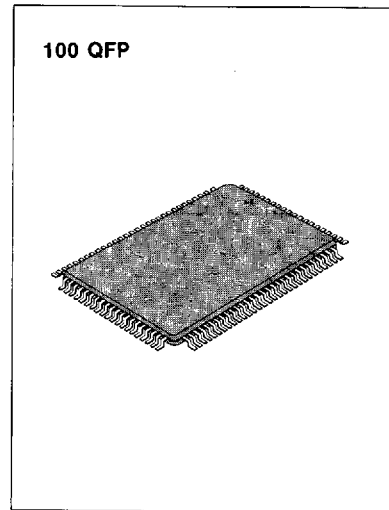
PIN CONFIGURATION

Fig. 2. 100 QFP Top View

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MAXIMUM ABSOLUTE LIMIT (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	$-0.3 \sim 6.0$	V
Driver supply voltage	V_{LCD}	$0 \sim 30$	V
Input voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Operating temperature	T_{opr}	$-20 \sim +85$	°C
Storage temperature	T_{stg}	$-55 \sim +150$	°C

Voltage greater than above may result in damage to the circuit.
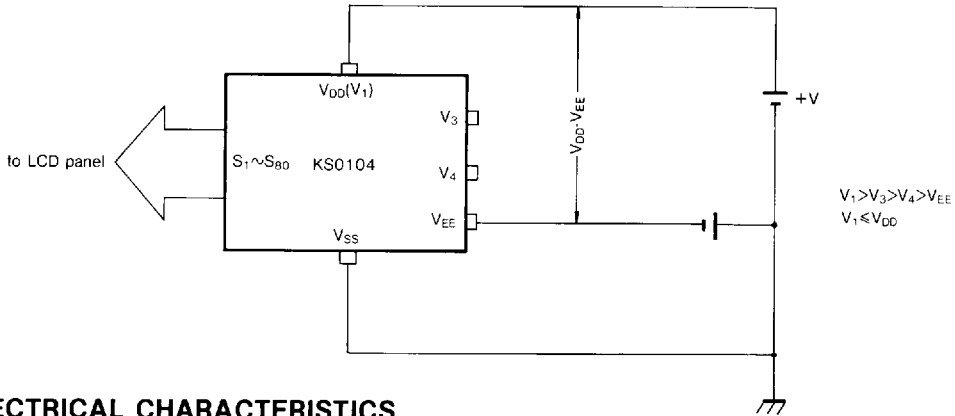
ELECTRICAL CHARACTERISTICS

DC Characteristics ($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=25°C, $C_L=15pF$)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Operating Voltage	V_{DD}	—		4.5	—	5.5	V
	$V_{DD}\text{-}V_{EE}$	—		8	—	28	
Input Voltage (*1)	V_{IH}	—		$0.8V_{DD}$	—	—	
	V_{IL}	—		—	—	$0.2V_{DD}$	
Input Current (*1)	I_{IH}	$V_{IH}=V_{DD}$, $V_{DD}=5.5V$		—	—	1	μA
	I_{IL}	$V_{IH}=0V$, $V_{DD}=5.5V$		—	—	−1	
Output Voltage (*2)	V_{OH}	$I_O=-0.2mA$, $V_{DD}=4.5V$		$V_{DD}-0.4$	—	—	V
	V_{OL}	$I_O=0.2mA$, $V_{DD}=4.5V$		—	—	0.4	
On resistance (*3)	R_{ON}	$V_{DD}\text{-}V_{EE}=23V$, $V_{DD}=4.5V$ *4|Vn-Vol|=0.25V		—	2	4	kΩ
Supply current (*5)	I_{DDSBY}	CL2=1MHz	Display data is not processing	—	—	200	μA
	I_{DDI}	$V_{DD}=5.5V$	Display data is processing	—	—	3	mA
	IV	$V_{DD}\text{-}V_{EE}=26V$	Current on V_1, V_3, V_4 V_{EE} pins	—	—	±100	μA
Input capacitance	CI	f=1MHz		—	5	—	pF

*1; Applicable pin; CL_1 CL_2, EI, E0, D_0-D_3 SHL, $\overline{DISPOFF}$, M
*2; Applicable pin; EI, EO
*3; Applicable pin; S_1-S_{80}
*4; $V_n=V_{DD}\text{-}V_{EE}$, $V_3=13/15$ ($V_{DD}\text{-}V_{EE}$), $V_4=2/15$ ($V_{DD}\text{-}V_{EE}$), $V_{DD}=V_1$
*5; Display data 1010-M=40Hz.

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AC CHARACTERISTICS (V_{DD}=+5±10%, V_{SS}=0V, T_a=+25°C, C_L=15pF)

Caracteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Clock frequency	f_{CL}	Duty=50%		3.4	—	—	MHz
Clock, pulse width	t_W			100	—	—	
Clock rise/fall time	f_{CT}			—	—	50	
Data set-up time	t_{SU}			50	—	—	
Data hold time	t_{DH}			80	—	—	
Clock-CL_1 time	t_{CL}			200	—	—	
CL_1 set-up time	t_{CSU}			90	—	—	ns
CL_1-clock time	t_{CK}			200	—	—	
Propagation delay time	t_{PHL}	$\overline{EO}$ Output		—	—	224	
		$\overline{EI}$ Output				224	
EO, EI set-up time	t_{PSU}	$\overline{EO}$ Input		70	—	—	
		$\overline{EI}$ Input		70			
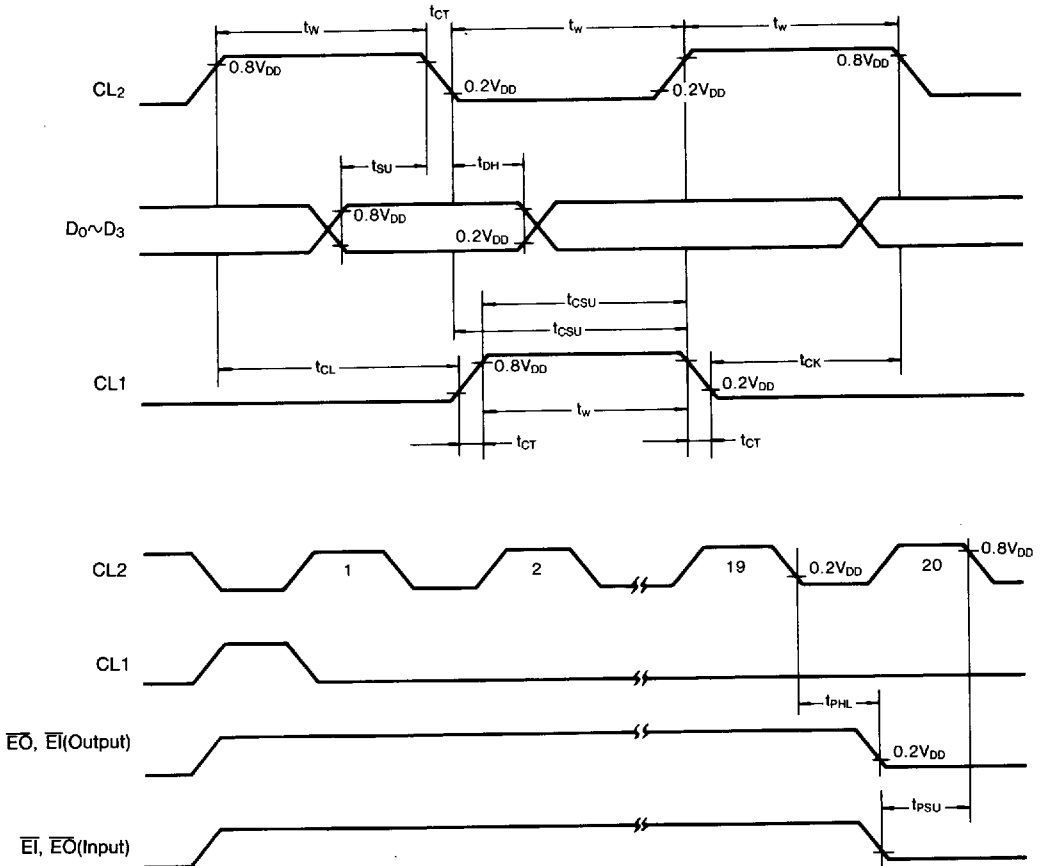
Fig. 3. Timing characteristic

PIN DESCRIPTION

Pin(No)	Input output	name	Function	Interface
$V_{DD}(40)$		Power supply	For logical circuit (+5V±10%)	Power
$V_{SS}(42)$			0V (GND)	
$V_{EE}(33)$			For LCD drive circuit	
V_1, V_3 $V_4,$ (34-36)	Input	LCD driver output voltage level	Bias supply voltage terminals to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. (refer to note I)	Power
$S_1 \sim S_{80}$ (1-30, 51-100)	output	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V_1, V_3, V_4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to; note 2)	LCD
CL2 (47)	input	data shift clock	Clock pulse input for the 4 bit parallel shift register. The data is shifted to 80 bit shift register at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE F/F is not active condition, is invalid.	controller
M (38)	input	alternate signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input	controller
CLI (49)	input	data latch clock	The signal for latching the shift register contents is input to this terminal. CL1 pulse "H" level initializes ENABLE F/F.	controller
$\overline{DISPOFF}$ (39)	input	output level control	Control input pin for display data output level ($S_1 \sim S_{80}$). V_1 level is output from $S_1 \sim S_{80}$ terminal during "L" level input. LCD becomes non-selected by V_1 level output from every output of segment drivers and every output of common drivers.	controller
SHL(41)	Input	Data interface		
$\overline{EO}$, $\overline{EI}$ (31,50)	Input Output		$\overline{EO}$ and $\overline{EI}$ can be used as either input terminal or output terminal according to the condition of SHL. The shifting direction of each data, $D_0 \sim D_3$, the I/O condition of $\overline{EO}$ and $\overline{EI}$, and the condition of SHL are described in the table below. (refer to note 3)	

| pin	I/O	SHL	Display data shift direction	Description
$\overline{EO}$	Input		D_0; $S_1 \rightarrow S_5 \rightarrow S_{77}$ D_1; $S_2 \rightarrow S_6 \rightarrow S_{78}$	Input terminal to ENABLE F/F of KS0104
$\overline{EI}$	Output	L	D_2; $S_3 \rightarrow S_7 \rightarrow S_{79}$ D_3; $S_4 \rightarrow S_8 \rightarrow S_{80}$	Output terminal of ENABLE F/F. $\overline{EI}$ is connected to next KS0104's $\overline{EO}$ when the KS0104's are connected in series (cascade connection)
$\overline{EI}$	Input		D_0; $S_{80} \rightarrow S_{76} \rightarrow S_4$ D_1; $S_{79} \rightarrow S_{75} \rightarrow S_3$	Input terminal to ENABLE F/F of KS0104
$\overline{EO}$	Output	H	D_2; $S_{78} \rightarrow S_{74} \rightarrow S_2$ D_3; $S_{77} \rightarrow S_{73} \rightarrow S_1$	Output terminal of ENABLE F/F. $\overline{EO}$ is connected to next KS0104's $\overline{EI}$ when the KS0104's are connected in series (cascade connection)

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PIN DESCRIPTION (continued)

Pin(No)	Input Output	name		Function		Interface
		PIN	I/O	SHL	Data direction	
		EO	Input	L		
		EI	Output			
		EI	Input	H		
		EO	Output			
D0~D3 (43-46)	Input	Display data input		Display data input pins for 4 bit parallel shift register and its is input synchronized with the clock pulse. The combination of D0~D3 level, M signal, Display data output level and the display on the LCD panel is described on the table below.(DISPOFF=H)		controller

D0~D3	M	Display data output level	Display on the LCD
L	L	V_3	OFF
H	L	V_1	ON
L	H	V_4	OFF
H	H	V_{EE}	ON

*NOTE 1

The below figure shows when the bias voltage is divided by the resistor (1/15 Bias, 1/200 Duty)

V1, VEE	Selection level
V3, V4	Non-selection level
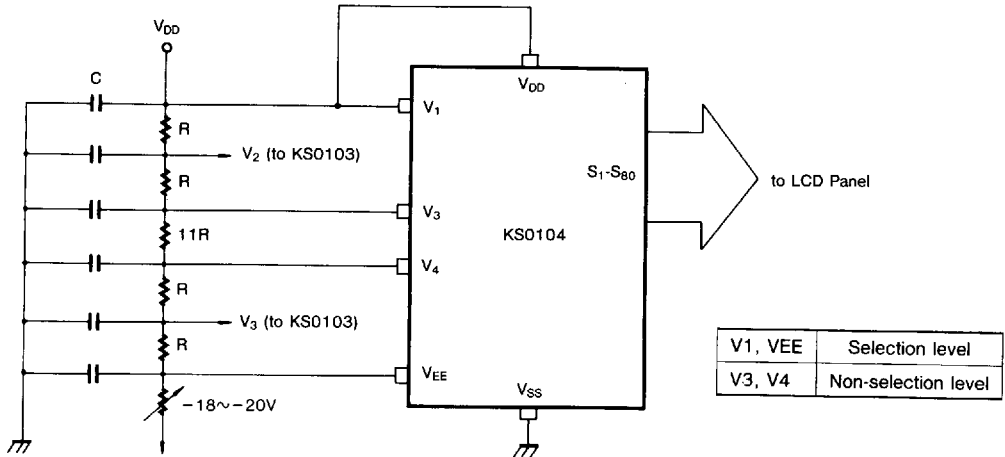
*NOTE 2 Truth table

M	Latched data	$\overline{\text{DISPOFF}}$	Output level (S$_1$-S$_{80}$)
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	VEE
X	X	L	V1

***NOTE 3**

- EO and EI pins working as input terminals.
  ENABLE F/F stops Display Data In at "H" level input. ENABLE F/F starts Display data In at "L" level input.
- EO and EI pins working as output terminals.
  These terminals are set to the "H" level immediately after ENABLE F/F is initialized by the load pulse. Upon completion of 80-bit serial/parallel conversion using the shift clock input from the CL2 terminal, these terminals are then set to the "L" level.
  The operation of ENABLE F/F is terminated and held unchanged until the next load pulse is detected.
  (For cascade connection, refer to the application circuit drawing.)

POWER DOWN FUNCTION

In order to reduce the power consumption, in case of cascade connection, KS0104 has a "power down function".
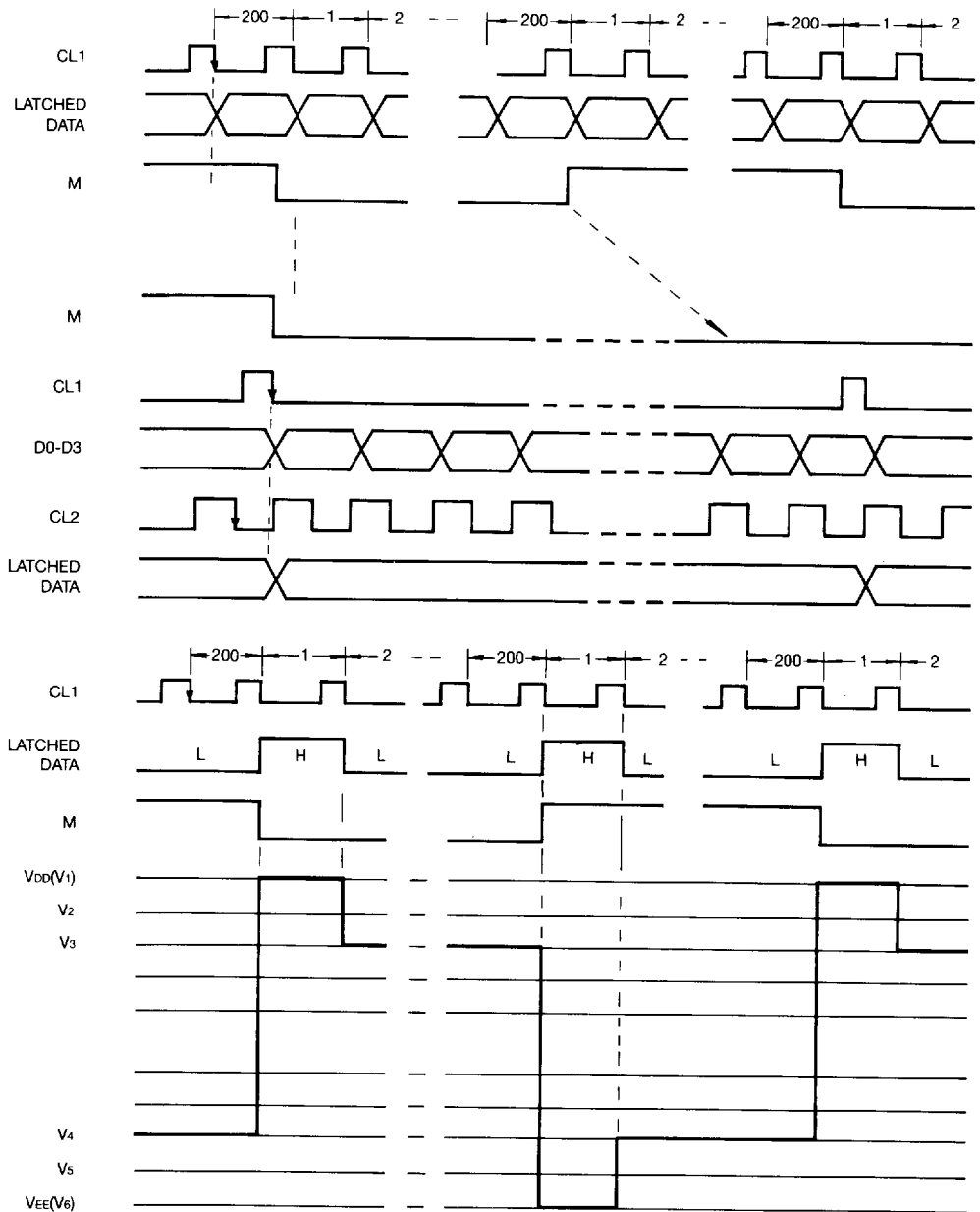
EI	Enable input	Enable	L
		Disable	H
EO	Enable output	EO of N th driver is connected to EI of (N+1) th driver KS0104	
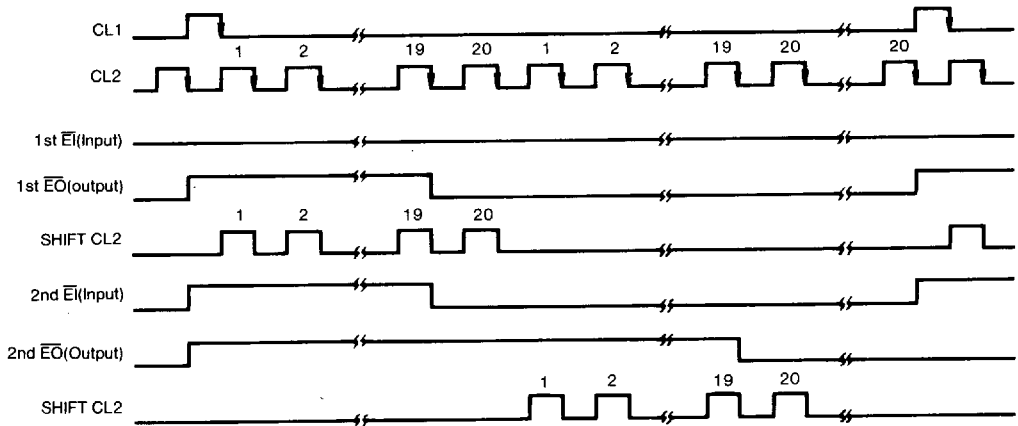
SHL = "H" (EI=Input EO=Output)
First KS0104's EO should be connected to second KS0104's EI.
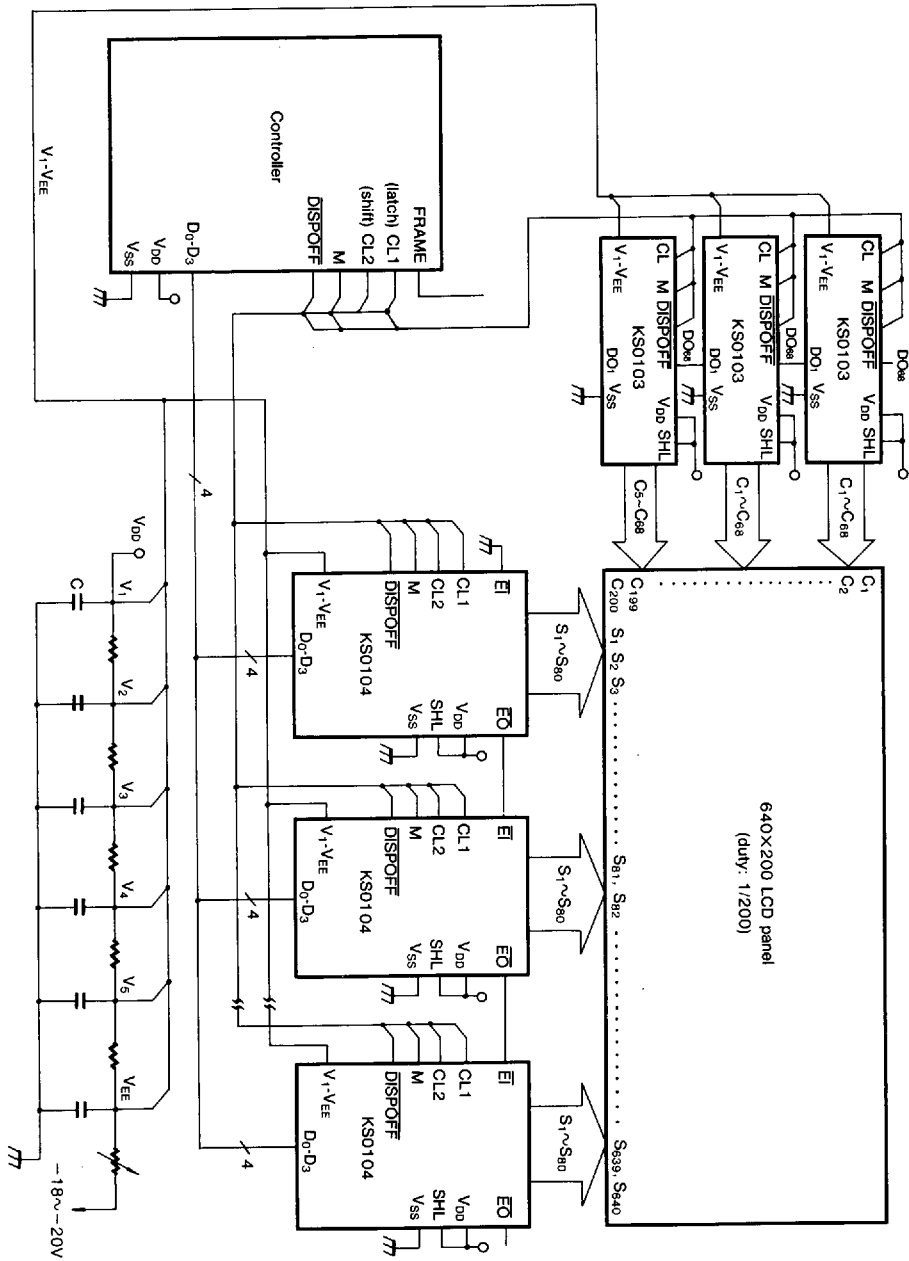
Fig 4. Timing Characteristics. (cascade connection)

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V1=VDD
V2=VDD-1/15 VLCD
V3=VDD-2/15 VLCD

V4=VDD-13/15 VLCD
V5=VDD-14/15 VLCD
VLCD=VDD-VEE

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APPLICATION CIRCUIT

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PACKAGE DIMENSIONS

60-QFP-1414A
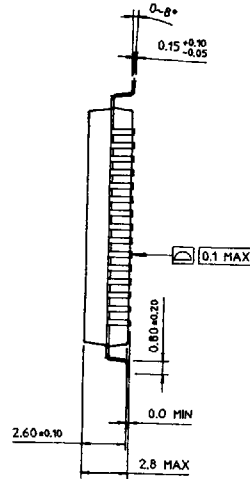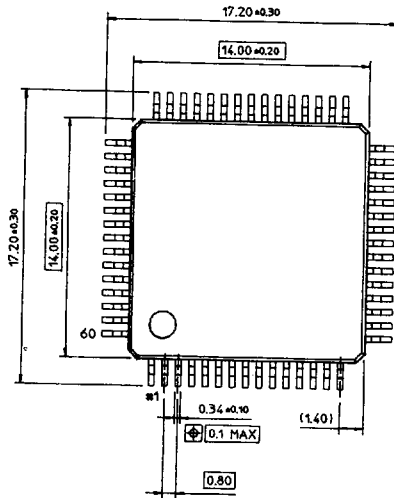
64-QFP-1420D
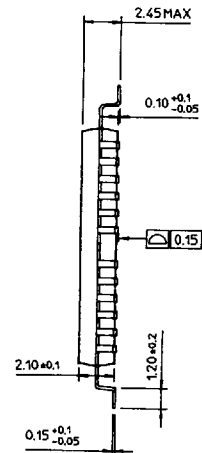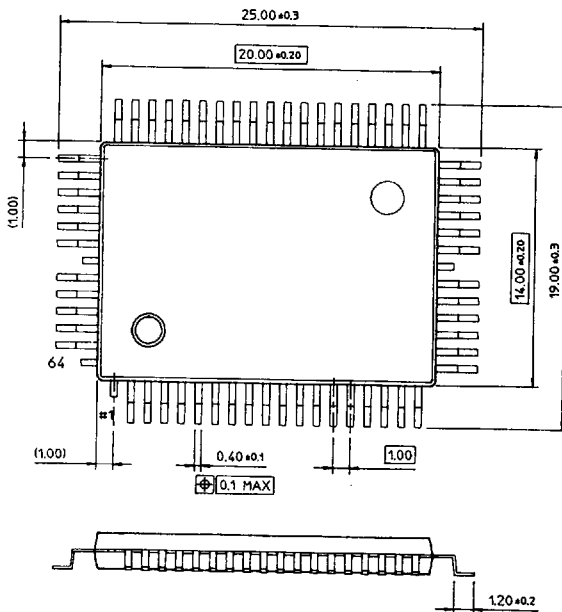
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PACKAGE DIMENSIONS

80-QFP-1420A

100-QFP-1420A
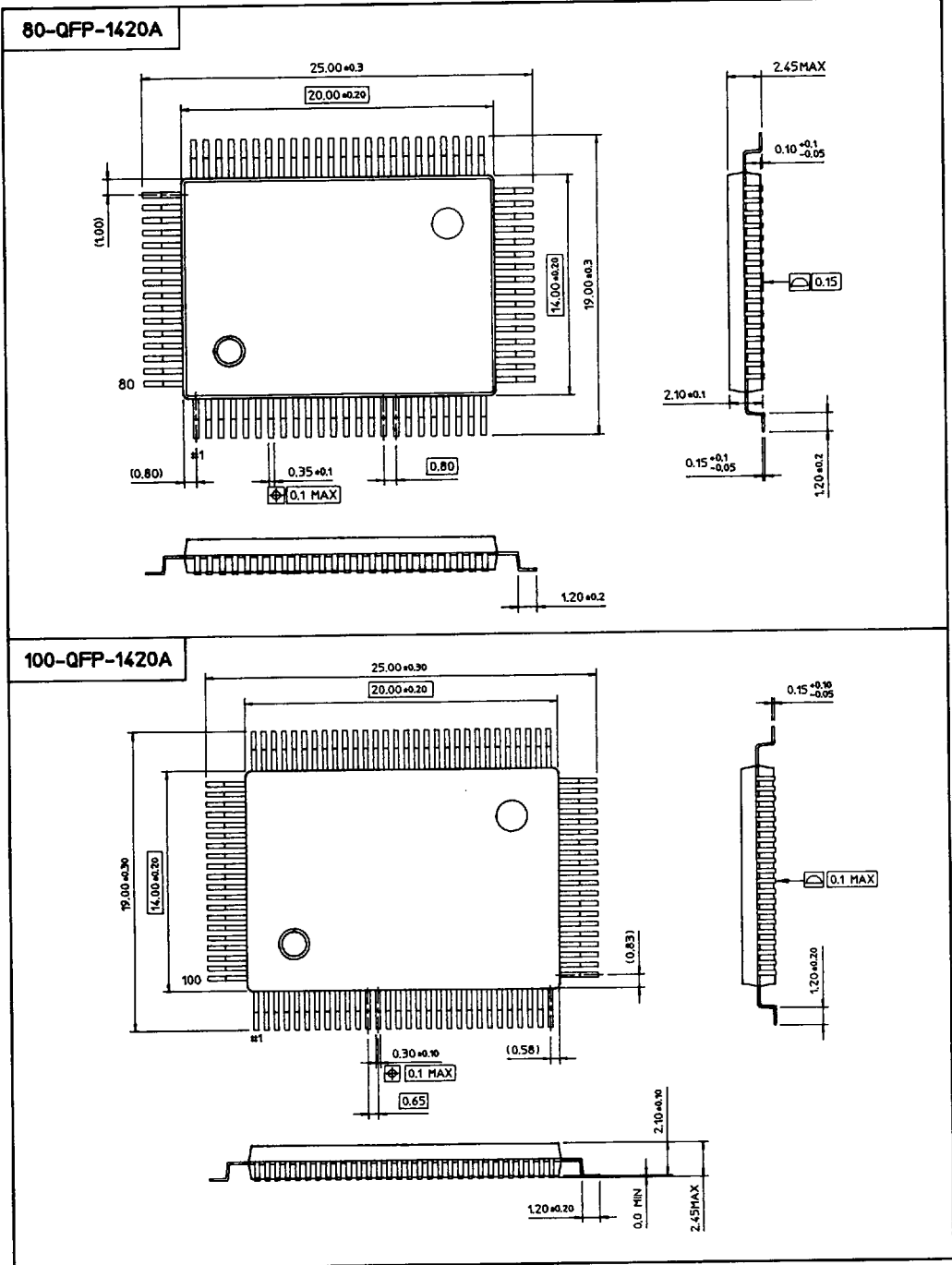
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PACKAGE DIMENSIONS

128-QFP-1420

98-TAB-35mm

3

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PACKAGE DIMENSIONS

98-STAB-35mm

35

0.80

1.20

1.71

1.90

KS0786

4.90

4.75

17.01

0.21BSC

1.00MAX

99-TAB-35mm

35

0.80MAX

0.24BSC

19.56

4.75

1.00

0.30

1.80 5.50 7.95

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PACKAGE DIMENSIONS

120-STAB-35mm

35

1.00

1.50

2.18

KS9769

2.90

4.20

4.75

0.23BSC

23.23

1.00MAX

3

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